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APPLICATION NO.	FILING DATE		FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/033,656	12/27/2001		Weimin Li	MICRON.076DV1	7957	
20995	7590	02/13/2004		EXAMINER		
		IS OLSON &	BROPHY, JAMIE LYNN			
2040 MAIN S FOURTEEN)R	ART UNIT	PAPER NUMBER		
IRVINE, CA	92614			2822		

DATE MAILED: 02/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application	n No.	Applicant(s)						
	10/033,656	10/033,656 LI, WEIMIN		•						
Office Action Summary		Examiner		Art Unit						
		J. L. Brophy	/	2822	pw					
The MAILING DATE f this	communication app	<u> </u>		orrespondence ac	Idress					
Period for Reply			. =\\=\====	0) 55014						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).										
Status										
1) Responsive to communicate	ion(s) filed on 11 De	ecember 20	<u>03</u> .							
2a) This action is FINAL .		action is no								
3) Since this application is in	condition for allowar	nce except f	or formal matters, pro	secution as to the	e merits is					
closed in accordance with	closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.									
Disposition of Claims										
4)⊠ Claim(s) <u>1-9</u> is/are pending	in the application.									
· · · · · · · · · · · · · · · · · · ·	4a) Of the above claim(s) is/are withdrawn from consideration.									
	Claim(s) is/are allowed.									
6)⊠ Claim(s) <u>1-9</u> is/are rejected										
7) Claim(s) is/are object	Claim(s) is/are objected to.									
8) Claim(s) are subject	to restriction and/or	r election re	quirement.							
Application Papers										
9) The specification is objected	d to by the Examine	r.								
10)⊠ The drawing(s) filed on <u>14 /</u>	10)⊠ The drawing(s) filed on <u>14 March 2003</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.									
Applicant may not request tha	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).									
Replacement drawing sheet(s	Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).									
11)☐ The oath or declaration is o	bjected to by the Ex	aminer. Not	e the attached Office	Action or form P	TO-152.					
Priority under 35 U.S.C. § 119										
12) ☐ Acknowledgment is made o	f a claim for foreign	priority und	er 35 U.S.C. § 119(a))-(d) or (f).						
a) ☐ All b) ☐ Some * c) ☐ None of:										
 Certified copies of th 	1. Certified copies of the priority documents have been received.									
2. Certified copies of the priority documents have been received in Application No										
3. Copies of the certified copies of the priority documents have been received in this National Stage										
application from the		•								
* See the attached detailed Of	fice action for a list	of the certifi	ed copies not receive	ed.						
Attachment(s)			4) []] Intended Outside	(DTO 442)						
 Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing 	Review (PTO-948)		4) Interview Summary Paper No(s)/Mail Da	ate						
3) Information Disclosure Statement(s) (P' Paper No(s)/Mail Date			5) Notice of Informal P 6) Other:	atent Application (PT	O-152)					

DETAILED ACTION

This office action is in response to the RCE and amendment filed 12/11/03.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/11/03 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2 and 4-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Marty et al (6,180,520).

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Marty et al teach an IC comprising a first planar network of electrical conductors

11, 12 formed in a first deposition process and providing a first electrical path of the circuit;

A second planar network of electrical conductors 21, 22 formed in a second deposition process, and providing a second electrical path of the circuit, the second planar network separated from the first planar network by a separation region; and

A single interlevel dielectric material 41 disposed within the separation region and extending into a portion of the first planar network without other intervening insulating materials between the first and second planar networks, the interlevel dielectric material 41 comprising polysiloxane, consisting essentially of silicon, oxygen, carbon and hydrogen and incorporating carbon-silicon bonding and having a dielectric constant of less than about 3.2 (col. 3, lines 29-34),

Wherein the planar networks 11, 12, 21, 22 comprise metal runners.

See Fig. 1 and accompanying text.

Fig. 1 depicts an IC comprising two interlevel dielectric materials 41, 42.

However, the second interlevel dielectric material 42 is optional (col. 3, lines 60-64).

Claims 1-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Aoi et al (5,877,080).

Aoi et al teach an IC comprising a first planar network of electrical conductors 24 formed in a first deposition process and providing a first electrical path of the circuit;

A second planar network of electrical conductors formed in a second deposition process, and providing a second electrical path of the circuit, the second planar network separated from the first planar network by a separation region (see, for example, col. 4, lines 1-8); and

A single interlevel dielectric material 21 disposed within the separation region and extending into a portion of the first planar network 24 without other intervening insulating materials between the first and second planar networks, the interlevel dielectric material comprising polysiloxane, consisting essentially of silicon, oxygen, carbon and hydrogen and incorporating carbon-silicon bonding and having a dielectric constant of less than about 3.2 (col. 10, lines 30-51),

Wherein the planar networks comprise metal runners, and

Wherein the interlevel dielectric material has a carbon content of between about 5% and 20% relative to a silicon content (col. 11, lines 13-17).

See, for example, Fig. 3(d) and accompanying text and col. 10, line 23 through col. 11, line 27.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

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Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marty et al in view of Gardener et al. (5,869,379) or Aoi et al in view of Gardener et al.

Marty et al and Aoi et al teach an IC that comprises an interlevel dielectric with a low dielectric constant as applied above to claims 1, 2 and 4-7 and claims 1-7, respectively. However, Marty et al and Aoi et al do not teach that the interlevel dielectric may be used as a sidewall spacer.

Gardener et al teaches a transistor with a sidewall spacer made of a low dielectric constant material (col. 2, lines 13-19) for the purpose of reducing the capacitive coupling between the gate conductor and adjacent source/drain regions.

Since Marty et al, Aoi et al and Gardener et al are from the same field of endeavor, the purpose disclosed by Gardener et al would have been recognized in the pertinent art of Marty et al and Aoi et al.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Marty et al or Aoi et al by using the low dielectric constant insulating layer as a sidewall spacer in a transistor structure because a person of ordinary skill in the art at the time the invention was made would have been motivated to lower the dielectric constant of the sidewall spacer in order to reduce capacitive coupling between the gate conductor and adjacent source/drain regions (see Gardener et al, col. 2, lines 21-25).

Response to Arguments

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Applicant's arguments filed 12/11/03 have been fully considered but they are not persuasive.

Applicant argues that Marty et al teach two interlevel dielectric materials between the first and second planar networks, and, therefore, do not teach the limitation of "without other intervening insulating materials between the first and second planar networks" (see p. 6 of arguments filed 12/11/03). However, as pointed out in the above rejection, the second interlevel dielectric material 42 taught by Marty et al is applied in a preferred embodiment (see Marty et al, col. 3, lines 60-64). Non-preferred embodiments constitute prior art (MPEP 2123).

Applicant argues that the Aoi structure includes a fluorine-silicon bond, and, therefore, Aoi does not teach the limitation of "consisting essentially of silicon, oxygen, carbon and hydrogen". Applicant specifically points out claim 1 of the Aoi reference which states that the interlevel dielectric material comprises a fluorine-silicon bond. However, Aoi et al teach other embodiments that do not comprise a fluorine-silicon bond (see, for example, Aoi et al, col. 10, lines 30-51).

Applicant argues that the horizontally separated elements disclosed in Gardner are not analogous to the vertically separated "planar networks" recited by Applicant. Further, Applicant argues that "Applicant has disclosed structures having a reduced dielectric constant without a cap layer, which relates only to vertically separated elements ("planar networks"), and is irrelevant to the horizontally separated elements taught by Gardner". If "planar networks" refers only to vertically separated elements,

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then claims 8 and 9 are not further limiting of independent claim 5 and should be canceled.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. L. Brophy whose telephone number is (571) 272-1835. The examiner can normally be reached on M-F (8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

J.J.B.

jlb